

Gain compensation

The invention relates to a device comprising a processing circuit with a predetermined limited dynamic range and an automatic gain control circuit, a method of automatic gain control, and an audio apparatus comprising such a device.

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US-A-5,389,927 discloses that automatic gain control (AGC) is typically used in a receiver to prevent saturation of one or more stages which saturation is caused by exceeding the dynamic range of a stage by a too large input signal. This prior art further discloses that applying AGC techniques to digital receivers as well to control front end gain 10 and digital gain is well known. The control of the front end gain overcomes the problem of insufficient dynamic range of the analog to digital converter (ADC) in digital receivers.

Further, US-A-5,389,927 discloses that in such a digital receiver with a front end which supplies an analog signal with a level depending on the signal strength received at the antenna, the ADC converts an analog input signal supplied by a front end into a digital 15 signal which is a digital representation of the analog signal. A detector detects the current signal amplitude of the digital signal and supplies a control signal to an amplitude controller which controls the amplitude of the analog input signal in steps to obtain a controlled analog signal which has an amplitude within the operating range of the ADC.

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It is an object of the invention to provide an automatic gain control which produces at an amplitude change of a controlled input signal due to an automatic gain control action, a signal amplitude of an output signal which better resembles the amplitude of the input signal.

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To this end, a device comprises a processing circuit with a predetermined limited dynamic range, and an automatic gain control circuit comprising:
a gain determining circuit for determining a first gain factor,
a first gain controller for controlling an amplitude of an input signal with the first gain factor to supply a gain controlled signal to the processing circuit,

a compensation circuit for determining a second gain factor based on the first gain factor and input parameters defining a time variation of the second gain factor, and

5 a second gain controller for receiving an output signal of the processing circuit and the second gain factor to obtain a compensated output signal being substantially compensated for an amplitude change of the gain controlled signal due to a change of the first gain factor.

The device with the automatic gain control circuit in accordance with the invention controls an amplitude of the input signal with a first gain factor to supply a gain controlled signal. The processing circuit processes the gain controlled signal into a processed signal. A second gain controller controls a gain of the processed signal with a second gain factor to obtain a compensated output signal which is substantially compensated for an amplitude change of the gain controlled signal due to a change of the first gain factor. The second gain factor is based on the first gain factor and input parameters which define a time variation of the second gain factor. Thus, when, at a particular instant, the first gain factor is changed, the second gain factor is adapted in such a way that the amplitude of the compensated output signal is substantially constant of course only if the input signal does not change during the transition period. In more general, the compensated output signal is compensated such that it better follows the input signal and thus is less disturbed by the variation of the first gain factor. This is especially important in audio applications. Any disturbance, even if temporarily only, of the amplitude of the compensated output signal will result in audible distortion of the signal. The first gain factor is supplied both to the automatic gain control circuit to change the amplitude of the input signal, and to the compensation circuit to indicate the instant and/or amount of the change of amplitude of the input signal.

The prior art US-A-5,389,927 controls the analog signal amplitude in factors of two. If the digital signal is controlled in factors of two in the opposite direction of the amplitude change of the controlled analog signal, the difference between the analog signal and the digital signal is reasonably small during the amplitude adaptations. However, the waveform of the digital signal temporarily deviates from the amplitude of the analog input signal when the amplitude of the controlled analog signal is changed. This causes an audible distortion every time the step change of the amplitude of the controlled analog signal is required. This audible distortion has to be filtered out which deteriorates the audio quality.

In an embodiment in accordance with invention, the processing circuit comprises an analog to digital converter ADC. The device with the automatic gain control circuit in accordance with the invention controls an amplitude of the analog input signal with

a first gain factor to supply a gain controlled analog signal. The first gain factor is determined such that the current signal amplitude of the digital signal does not exceed the input range of the ADC. The ADC converts the gain controlled analog signal into a digital signal. A second gain controller controls a gain of the digital signal with a second gain factor to obtain a
5 compensated digital signal which is substantially compensated for an amplitude change of the gain controlled analog signal due to a change of the first gain factor. The second gain factor is based on the first gain factor and input parameters which define a time variation of the second gain factor. Thus, the compensated digital signal is compensated such that it better follows the analog input signal and thus is less disturbed by the variation of the first gain
10 factor.

With the current signal amplitude of the digital signal is meant the maximum value the digital signal has or is expected to have. The bits of the digital signal word may be generated by the analog to digital converter directly in parallel, it is also possible that the analog to digital converter supplies the bits of the word serially.

15 In an embodiment in accordance with the invention, the gain control provides an input signal which fits within the operating range of the ADC and thus prevents that at a too large amplitude of the analog input signal will be clipped by the analog to digital conversion, or that a large part of the range of the ADC is not used.

20 In an embodiment in accordance with the invention, the first gain factor is adapted in steps, this is simpler than to cater for a continuously variable first gain factor.

In an embodiment in accordance with the invention, the first gain factor is changed in steps which are a power of two. This allows a change of the digital amplitude by bit-shifting, which is very simple.

25 In an embodiment in accordance with the invention, a delay circuit delays a start instant of the controlling of the amplitude of the output signal of the processing circuit. When the first gain factor is changed, the analog gain is adapted immediately. The second gain should however not be adapted immediately. It takes some time before the adaptation of the analog gain is noticeable in the output signal of the processing circuit. This delay is caused by a processing time of the processing circuit between the gain controlled signal and
30 the compensated digital signal. Thus, the second gain factor should start changing after this delay. If the processing circuit comprises an ADC, the second gain factor is also referred to as the digital gain factor.

In an embodiment in accordance with the invention, the compensation circuit comprises a waveform generation circuit which generates a waveform determining the time

variation of the second gain factor. If the first gain factor is changed with a step, the amplitude of the gain controlled signal will change with a step. However, the amplitude of the output signal of the processing circuit will not vary stepwise. The processing circuit (which may comprise an ADC and, optionally, other digital circuits such as digital filters)

5 cause the step variation of the gain controlled signal to become smeared out in time, for example due to bandwidth limitations. Thus, if an amplitude of the compensated signal is required which is less disturbed by the step variation of the gain controlled signal, the second gain should vary in time in accordance with a well defined waveform to compensate the smeared-out response.

10 In an embodiment in accordance with the invention, the waveform generating circuit comprises a bandwidth limitation circuit to obtain the smeared-out change of the second gain factor corresponding to the smear out effect of the processing circuit. It is also possible to approximate or obtain the same behavior by using a linear interpolation, or even better a higher order interpolation, or by using a table look-up or a line drawing algorithm.

15 In an embodiment in accordance with the invention, a static error is compensated for. If the first gain factor indicates that the amplitude of the analog signal should change a predetermined amount, actually a slight deviation from this predetermined amount might occur. It is not sufficient to compensate the amplitude of the output signal of the processing circuit with exactly the same predetermined amount. After the transition

20 period, when the delay and the waveform of the second gain factor are not important anymore, still a difference is present between the amplitude of the compensated signal and the original input signal. This difference is compensated for by the level adaptation circuit.

In an embodiment in accordance with the invention, a well known single bit sigma-delta analog to digital converter is used. Such an analog to digital converter is simple.

25 A further advantage is that the gain compensation operates on a single-bit signal instead of a multi-bit signal thus removing the need for an explicit multiplication.

In an embodiment in accordance with the invention, the digital gain is controlled at the ADC directly. An example of a suitable ADC is an ADC with a possibility to control its reference.

30 In an embodiment in accordance with the invention, the digital gain (the second gain factor) is controlled by a digital gain controller (the second gain controller) which processes the digital signal (the processed signal) supplied by the ADC. The ADC may now be of any kind.

In an embodiment in accordance with the invention, the processing circuit may comprise further digital processing (for example a digital filter). The gain compensation is obtained by controlling the amplitude of the processed digital signal supplied by the digital processing circuit.

5 In an embodiment in accordance with the invention, both the gain of the digital signal supplied by the ADC and the gain of the processed digital signal supplied by the digital processing circuit are controlled.

In an embodiment in accordance with the invention, an automatic calibration circuit performs during a test period, repeatedly the next operations:

10 generating a reference signal being supplied as the input signal,
adapting the first gain factor with a predetermined amount,
providing a first set of input parameters,
checking whether a change of amplitude occurs of the compensated output signal, and

15 adapting at least one of the input parameters, until substantially no change of amplitude occurs of the compensated output signal, and
finally storing the input parameters determined, for use during normal operation.

20 These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described by way of example in the following description and with reference to the accompanying drawings, in which

Fig. 1 shows a simple gain compensation circuit,

25 Fig. 2 shows signals for elucidating the operation of the gain compensation circuit shown in Fig. 1,

Fig. 3 shows a block diagram of the gain compensation circuit in accordance with an embodiment of the invention,

30 Fig. 4 shows signals for elucidating the operation of the gain compensation circuit shown in Fig. 3,

Fig. 5 shows a block diagram of the gain compensation circuit of an embodiment in accordance with the invention,

Fig. 6 shows a block diagram of the gain compensation circuit of an embodiment in accordance with the invention,

Fig. 7 shows a block diagram of the gain compensation circuit of an embodiment in accordance with the invention,

Fig. 8 shows an embodiment in accordance with the invention of a digital gain controller, and

5 Fig. 9 shows an embodiment in accordance with the invention of an automatic calibration circuit.

In the Figures, elements which correspond to elements described previously have the same reference numerals.

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Fig. 1 shows a simple gain compensation circuit. A gain circuit B3 receives a gain control signal referred to as gain factor g , an analog input signal S1 which has a certain dynamic range and bandwidth and supplies a gain controlled analog signal S3 to the analog to digital converter B1. The gain circuit B3 usually is an attenuating circuit. The attenuating 15 circuit may comprise a number of attenuators (indicated by $2^0, 2^{-1}, 2^{-n}$) which attenuate the analog input signal S1 with factors which are powers of the number 2. It is possible to use other factors. A multiplexer M1 selects the attenuator output signal(s) fitting the gain factor g . The ADC B1 converts the gain controlled analog input signal S3 into a digital signal S4.

A detection circuit B2 continuously checks the current signal level of the 20 digital signal S4 and compares this level to the maximum allowable input-level of the ADC B1. If the level of the digital signal S4 approaches the maximum allowable level, the detection circuit B2 adapts the gain factor g to obtain a same attenuation factor g of the gain circuit B3. The scaling of the ADC B1 output signal, which is the digital signal S4, introduced by the attenuating circuit B3 is later compensated by a digital gain controller B10 25 which amplifies the digital signal S4 by the same factor g to obtain a digital output signal S2 which has an amplitude which is as constant as possible.

For an efficient implementation of the digital gain controller B10, often the attenuating circuit B3 comprises the above mentioned set of fixed attenuation factors which are powers of 2, which thus gives rise to attenuation in multiples of 6dB. The digital gain 30 controller B10 increases the amplitude of the digital signal S4 in steps of 6dB by simply shifting the bits of the digital word by one bit. In fact, more generally, the attenuation-factor g determines an attenuation-factor (the powers of 2 indicated in the digital gain controller B10) selection (by the multiplexer M2) in the digital gain controller B10.

The switching of the attenuation factor g of the attenuating circuit B3 happens almost instantaneously, resulting in a step-wise amplitude change in the gain controlled analog signal S3. Due to the bandwidth limitation inherently present in the system, for example, due of the ADC B1, this step is spread out, and after some delay TD (see Fig. 2) the 5 step results in a relatively slow transient TR of the digital signal S4. In addition to the delay TD and the transient TR, there is a setting-dependent deviation E from the ideal attenuation due to process-spread and non-idealities in the analog design. In this simple gain compensation circuit, the attenuation is compensated by a step and the digital output signal S2 is temporarily distorted. This is illustrated with respect to Fig. 2.

10 Depending on the application, all these distortions result in unwanted and noticeable artifacts. For example, in case of AM-reception, these distortions give rise to a click-noise in the output audio signal which either has to be filtered out or muted, and thus leads to inferior audio quality. This effect becomes worse if the AGC switches periodically or with a certain periodicity.

15 Fig. 2 shows signals for elucidating the operation of the simple gain compensation circuit. Fig. 2A shows the gain factor g which increases almost stepwise at instant t_1 . This indicates to the gain circuit B3 that the amplitude of the gain controlled analog signal S3 should decrease a predetermined amount, and to the digital gain controller B10 to increase the amplitude of the digital signal S4 with the same predetermined amount.

20 Fig. 2B shows the stepwise decrease of the amplitude of the gain controlled analog signal S3. Fig. 2C shows the change of the digital signal S4 in response to the step of the amplitude of the gain controlled analog signal S3. The amplitude of the digital signal S4 starts decreasing at an instant t_2 which is a delay time TD later than instant t_1 at which the gain controlled analog signal S3 decreases. During a transition period TR (also referred to as the transition

25 TR), the amplitude of the digital signal S4 decreases to its final level. The final level which is reached at instant t_3 may have an offset or error E with respect to the expected level. Fig. 2D shows the compensated digital signal S2. The gain factor g of Fig. 2A corrects the digital signal S4 by enlarging the gain of the digital gain controller B10 at the instant t_1 at which the digital signal S4 is not changed due to the stepwise change of the gain controlled analog

30 signal S3. Consequently, the amplitude of the compensated digital signal S2 is too large. At instant t_2 the too large amplitude of the compensated digital signal S2 starts decreasing due to the decreasing amplitude of the digital signal S4. After instant t_3 , the desired level DL is reached, only the error E will still be present.

Due to the imperfect compensation, a much too high amplitude of the compensated digital signal occurs from instant t_1 to instant t_3 . This distortion will be audible in audio systems. A much too low amplitude of the compensated digital signal will occur if the step occurs in the other direction.

5 Fig. 3 shows a block diagram of the gain compensation circuit in accordance with an embodiment of the invention.

The gain circuit B3 receives a gain control signal referred to as gain factor g , and an analog input signal S1, and supplies a gain controlled analog signal S3 to the analog to digital converter B1. The gain circuit B3 may be identical to the gain circuit B3 described 10 with respect to Fig. 1. The ADC B1 converts the gain controlled analog input signal S3 into a digital signal S4.

A detection circuit B2 continuously checks the current signal level of the digital signal S4 and compares this level to the maximum allowable input-level of the ADC B1. If the level of the digital signal S4 approaches the maximum allowable level, the 15 detection circuit B2 adapts the gain factor g to obtain a same attenuation factor g of the attenuating circuit B3. The scaling of the ADC B1 output signal, which is the digital signal S4, introduced by the attenuating circuit B3 is later compensated by a digital gain controller B10. A compensation circuit B5 determines a digital gain factor dg based on both the gain factor g which comprising information on when the gain factor is changed and by how much 20 and on parameters DL, TR, DV which determine the variation in time of the digital gain factor dg . The digital gain controller B10 controls the gain of the digital signal S4 with a factor determined by the digital gain factor dg to obtain a digital output signal S2 which has an amplitude which is substantially constant or more precisely defined if the input signal is varying: an amplitude which is substantially undisturbed.

25 The main idea of the compensation circuit in accordance with a preferred embodiment of the invention is to implement a gain compensation which substantially perfectly compensates for the non-idealities described with respect to the simple compensation as elucidated with respect to Figs. 1 and 2. In principle the substantially perfect compensation is obtained by means of time-varying the gain of the digital gain controller B10 30 in such a way that the artifacts in the compensated digital signal S2 are substantially removed.

The compensation circuit B5 generates a digital gain factor dg which is complementary to all the distortions seen at the point in the processing chain where the gain compensation is performed. This digital gain factor dg is used as a compensation signal for

the digital gain controller B10. In principle, in a preferred optimal compensation scheme, the digital gain factor dg is determined based on the gain factor g , the delay TD , the transition characteristics of the transition TR and the error E . The compensation circuit B5 thus generates a digital gain dg with a programmable delay, start-gain, end-gain and transition characteristics. The digital gain in accordance with the invention thus is not just a step-wise compensation which occurs coincident with the change of the gain factor, but has at least either a delay, a changing value, or on static error compensation component.

5 The digital gain controller B10 may be identical to the one described with respect to Fig. 1.

10 Fig. 4 shows signals elucidating the operation of the gain compensation circuit shown in Fig. 3. Fig. 4A shows the gain factor g which switches from attenuation factor g_k to g_i at instant t_1 . The gain controlled analog signal S_3 which is the ADC B1 input signal almost immediately responds to the new setting of the attenuating circuit B3 as is shown in Fig. 4B. This new setting deviates with a setting depending deviation E from the ideal 15 attenuation. The analog to digital conversion by the ADC B1 introduces a processing delay TD . The gain compensation circuit B5 generates the digital gain factor dg as shown in Fig. 4D. The digital gain factor dg starts increasing at instant t_2 which is the delay time TD later than the instant t_1 . The digital gain factor dg increases until the instant t_3 along a curve which is complement to the corresponding curve of the amplitude error of the digital signal S_4 if not 20 compensated. After instant t_3 , the digital gain factor dg has a value suitable to compensate for the error E . The distortions are substantially perfectly compensated in the compensated digital signal S_2 as shown in Fig. 4E. It is not required that all the aspects are compensated. The compensated digital signal S_4 has a less distorted amplitude than in the prior art even when the error E is not or not fully compensated. It is also not required to perfectly 25 compensate during the transition period. A rough estimation of the optimal curve during the transition period will improve the behavior of the compensation circuit over the prior art. An improvement over the prior art is obtained also when at least one of the effects of delay time TD , the transition period TR , or the error E is compensated to at least some extend.

30 The shape of the curve of the digital gain dg during the transition period TD may be obtained by linear interpolation of two or more value/time pairs which preferably are obtained from a memory (not shown). A better accuracy may be reached by using a higher order interpolation. Alternatively, well known methods like table look-up or line-drawing algorithms can be used depending on a trade-off between accuracy and effort.

Preferably, all the parameters determining the variation of the digital gain factor dg during the transition period TR, the duration of the delay period TD, and the setting-dependent deviation or error E are user programmable.

Fig. 5 shows a block diagram of an embodiment in accordance with the 5 invention of the gain compensation circuit.

The gain circuit B3 receives a gain control signal referred to as gain factor g, an analog input signal S1 and supplies a gain controlled analog signal S3 to the analog to digital converter B1. The ADC B1 further comprises an input to receive the digital gain factor dg and converts the gain controlled analog input signal S3 into a gain compensated 10 digital signal S2. A detection circuit B2 continuously checks the current signal amplitude of the compensated digital signal S2 and/or the gain controlled analog signal S3 to determine the gain factor g. A compensation circuit B5 determines the digital gain factor dg based on the gain factor g, and the parameters for the duration of the delay period TD, for the shape of the gain variation during the transition period TR, and the error E.

15 This digital gain control in the ADC B1 is in particular relevant for ADC's of which the reference can be controlled.

Fig. 6 shows a block diagram of an embodiment in accordance with the invention of the gain compensation circuit.

The controllable variable gain circuit B3 receives the gain factor g, the analog 20 input signal S1 and supplies the gain controlled analog signal S3 to the analog to digital converter B1 which converts the gain controlled analog signal S3 into a digital signal S4. A detection circuit B2 continuously checks the current signal amplitude of the digital signal S4 and/or the gain controlled analog signal S3 to determine the gain factor g. A digital processing circuit B11 receives the digital signal S4 and supplies the processed digital signal 25 S5 to the digital gain controller B10 to obtain the compensated digital signal S2. The compensation circuit B5 determines the digital gain factor dg based on the gain factor g, and the parameters for the duration of the delay period TD, for the shape of the gain variation during the transition period TR, the error E, and the processing in the processing circuit B11. The digital gain factor dg is supplied to the digital gain controller B10 to control the 30 amplitude of the processed digital signal S5. The digital processing circuit B11 may perform decimation filtering.

The compensation of the gain variation by the gain circuit B3 in the analog domain is compensated in the digital domain behind the digital processing circuit B11. This has the advantage that if the digital processing circuit B11 comprises a sample rate down-

converter, or a decimation filter that the compensation is performed on a signal with a lower sample rate.

Fig. 7 shows a block diagram of an embodiment in accordance with the invention of the gain compensation circuit.

5 The controllable variable gain circuit B3 receives the gain factor g , the analog input signal S1 and supplies the gain controlled analog signal S3 to the analog to digital converter B1 which converts the gain controlled analog input signal S3 into a digital signal S4. A detection circuit B2 continuously checks the current signal amplitude of the digital signal S4 and/or the gain controlled analog signal S3 to determine the gain factor g . A digital
10 gain controller B12 receives the digital signal S4 to supply an intermediate compensated digital signal S6. A digital processing circuit B11 receives the intermediate compensated digital signal S6 and supplies the processed digital signal S5 to the digital gain controller B10 to obtain the compensated digital signal S2. A compensation circuit B14a determines the digital gain factor dga based on the gain factor g , and the parameters for the duration of the
15 delay period TD, for the shape of the gain variation during the transition period TR, and the error E. The digital gain factor dga is supplied to the digital gain controller B12 to control the amplitude of the digital signal S4. A compensation circuit B14b determines the digital gain factor dgb based on the gain factor g , and the parameters for the duration of the delay period TD, for the shape of the gain variation during the transition period TR, the error E, and the
20 processing of the processing circuit B11. The digital gain factor dgb is supplied to the digital amplifier B10 to control the gain of the processed digital signal S5.

Now the compensation of the gain variation by the gain circuit B3 in the analog domain is compensated in the digital domain partly directly behind the ADC B1 and partly behind the digital processing circuit B11. This has the advantage that if the digital
25 processing circuit B11 comprises a sample rate down-converter, or a decimation filter that the compensation is performed on a signal with a lower sample rate.

Fig. 8 shows an embodiment in accordance with the invention of a compensation circuit.

The compensation circuit B5 or B14a, B14b comprises a delay circuit B6, a
30 waveform generating circuit B7, a level adaptation circuit B8 and a combining circuit B9.

The delay circuit receives B6 the gain factor g and a delay parameter DL to supply the delay time TD. The delay time TD indicates an instant a delay time TD later than the instant at which the gain factor g changes. The duration of the delay time TD is determined by the delay parameter DL. The delay parameter may be stored in memory.

The waveform generating circuit B7 receives the gain factor g and at least one waveform parameter WP defining the waveform information WF according which the digital gain dg has to vary during the transition period TR. The waveform generating circuit B7 may receive timing information TI from the delay circuit B6 which at least indicates the start of

5 the transition period. The waveform parameter WP may comprise the timing information on the duration of the transition period and also on the start of the transition period with respect to the instant the gain factor g changes. The waveform parameter WP further comprises one or more values determining the desired waveform information WF. The gain factor g provides information on the required amount the digital gain dg should vary, and on the

10 instant the gain in the analog domain is changed. However, this timing instant may not be used as it may be present in the timing information TI. The waveform generating circuit B7 may receive information on a correction required to compensate for the influence of a processing circuit B11 if present.

The level adaptation circuit B8 receives a delta gain factor DV and the gain

15 factor g to determine the amount the digital gain dg has to change, and on the instant the gain in the analog domain is changed. The delta gain factor DV indicates the value for the offset or error information E required to obtain a perfect compensation after the transition period TR. The timing information (obtained from the gain factor g or from the delay circuit B6) may be used to activate this compensation during or after the transition period TR.

20 The combining circuit B9 combines the delay parameter DL, the waveform information WF and the error information E to obtain the time-varying digital gain or digital gain factor dg .

Fig. 9 shows an embodiment in accordance with the invention of an automatic calibration circuit. The circuit shown in Fig. 9 is based on the circuit shown in Fig. 3. An

25 automatic calibration circuit B13 and a switch SW are added. The automatic calibration circuit B13 receives the compensated digital signal S2, and supplies: a switch control signal SWS to the switch SW, the parameters DL, TR, and OV to the compensation circuit B5, and a control signal AG to the gain circuit B3 and the compensation circuit B5.

During a calibration period, the automatic calibration circuit B13 first sets the

30 parameters DL, TR and OV. Secondly, the automatic calibration circuit B13 supplies a reference signal RS with a predetermined level as the analog signal S1 to the controllable variable gain circuit B3 because the switch SW is in the position shown. Then, the automatic calibration circuit B13 provides the information AG to the gain circuit B3 and the compensation circuit B5 to indicate the instant at which the gain of the gain circuit B3 and

the digital gain controller B10 has to be changed. Instead of supplying the information AG directly to the gain circuit B3 and the compensation circuit B5, the information AG may also control the gain factor g. Now, the automatic calibration circuit B13 evaluates the amplitude of the compensated digital signal S2.

5 If the amplitude of the compensated digital signal S2 is sufficiently constant in time, the parameters DL, TR and OV used are stored and normal operation is resumed. During normal operation, the switch SW is in the position not shown in Fig. 9 and the automatic calibration circuit is inactive.

10 If the amplitude of the compensated digital signal S2 is not sufficiently constant in time, the automatic calibration circuit B13 varies one or more of the parameters DL, TR and OV and restarts a calibration cycle. The automatic calibration circuit B13 repeats the calibration cycle as often as required to obtain a substantially constant compensated digital signal S2 in response to a change of the gain factor g. At the end of the last calibration cycle the optimal parameters DL, TR and OV found are stored for use during the normal 15 operation phase.

Many strategies can be used to find the optimal parameters DL, TR and OV. For example, by determining at which instant the compensated digital signal deviates from the required level. For example, when a deviation occurs near to the instant the gain factor g is changed, the parameter DL should be adapted to get a longer delay time TD, if a long time 20 after this instant an error is present, the parameter OV should be changed to lower the error E. The remaining error can be minimized by sampling the deviation during the transition period and by using the sampled values in the parameter TR.

The general context of this invention is the technique of automatic gain control in combination with analog to digital converters used in various kinds of applications, e.g. 25 radio receivers, wire-line communication, data transceivers etc.

An example of an implementation is elucidated in the now following. The compensation circuit or the corresponding compensation method described has been implemented in hardware on a test-chip in the context of a digitally implemented analog broadcast AM/FM radio receiver for car-radio applications. For a hardware-efficient solution 30 a single-bit sigma-delta ADC is used. The test-chip comprises a set of 4 attenuator settings. The digital gain compensation is performed as early as possible in the system, which is immediately on the bit-stream of the ADC. This has the advantage of low hardware effort since the gain compensation operates on a single signal-bit instead of a multi-bit-bus thus removing the need for explicit multiplication. To compensate during the transient period TR,

linear interpolation showed to provide good performance in that the remaining disturbances were not audible. The user programmable parameters DL, TR and OV are the duration of the delay period TD, the slope of the linear interpolated waveform of the digital gain during the transition period TR, and four attenuator setting dependent gain deviations E, respectively.

5 This method of compensation can be used, for example, in the following applications: in general applications which use an ADC and stepped AGC's, in integrated circuits for e.g. car-radio, cellular phones, portable radio etc. RF-, LF-, and baseband-processing, and in audio (HiFi-) equipment. The method of compensation is also useful in systems without an ADC. Usually, processing circuits are used which have a limited dynamic
10 range. Often the dynamic range is limited by the power supply voltages applied. In particular if circuits are integrated in an integrated circuit, the dynamic range of these circuits may be quite limited due to relatively low supply voltages. The amplitude of the input signal of such processing circuits is controlled by a first gain control circuit preceding the processing circuit. The effect of the first gain control circuit is substantially compensated by providing a
15 second gain control circuit operating on the output signal of the processing circuit to restore the amplitude of the output signal.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims.

20 In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. Use of the verb "comprise" and its conjugations does not exclude the presence of elements or steps other than those stated in a claim. The article "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention may be implemented by means of hardware comprising several distinct elements,
25 and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means may be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.